IN THE CLAIMS:

Listing of claims:

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1. (currently amended) A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a ~~cell~~ first capacitor formed in a DRAM region of a semiconductor substrate, and a second capacitor ~~element~~ formed in an analog element region of the semiconductor substrate, the method comprising the steps of:

(a) simultaneously forming a storage node of the ~~cell~~ first capacitor and a lower electrode of the second capacitor ~~element~~;

(b) simultaneously forming a dielectric layer of the ~~cell~~ first capacitor and a dielectric layer of the second capacitor ~~element~~; and

(c) simultaneously forming a cell plate of the ~~cell~~ first capacitor and an upper electrode of the second capacitor ~~element~~.

2. (original) A method for manufacturing a semiconductor device according to claim 1, further comprising, before the step (a), the step of simultaneously forming

a word line that is a component of the DRAM and

a connection layer that is located in a common layer of the word line and that electrically connects the lower electrode to another element in the semiconductor device.

3. (original) A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region

where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

4. (original) A method for manufacturing a semiconductor device according to claim 2, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

5. (original) A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein an impurity is diffused in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

6. (original) A method for manufacturing a semiconductor device according to claim 2, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried simultaneously with step (c), and

wherein an impurity is diffused in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

7. (original) A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) carried out simultaneously with step (c), and

wherein a silicide layer is formed in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

8. (original) A method for manufacturing a semiconductor device according to claim 2, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region,

wherein the step (d) is carried out simultaneously with step (c), and

wherein a silicide layer is formed in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

9-14. (canceled)

15. (currently amended) A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a ~~cell~~ first capacitor formed in a DRAM region of a semiconductor substrate, and a second capacitor ~~element~~ formed in an analog element region of the semiconductor substrate, the method comprising:

forming a first conducting layer and etching a portion of the first conducting layer to form a storage node of the ~~cell~~ first capacitor and a lower electrode of the second capacitor ~~element~~;

forming a dielectric layer and etching a portion of the dielectric layer to form a dielectric layer region of the ~~cell~~ first capacitor and a dielectric layer region of the second capacitor ~~element~~; and

forming a second conducting layer and etching a portion of the second conducting layer to form a cell plate of the ~~cell~~ first capacitor and an upper electrode of the second capacitor ~~element~~.

16. (currently amended) A method according to claim 15, further comprising, prior to forming the storage node of the ~~cell~~ first capacitor and the lower electrode of the second capacitor ~~element~~, forming an additional conducting layer and etching the additional conducting layer to form a word line that is a component of the DRAM and to form a connection layer that is located in a common layer of the word line and that is configured to electrically connect the lower electrode to another element in the semiconductor device.

17. (original) A method for manufacturing a semiconductor device according to claim 15, wherein the etching a portion of the second conducting layer also forms a first resistance element and a second resistance element in the analog element region, and wherein the first resistance element and second resistance element are formed with a resistance value of the first resistance element being lower than that of the second resistance element.

18. (original) A method for manufacturing a semiconductor device according to claim 1, further comprising the step of:

(d) forming a first resistance element and a second resistance element in the analog element region, wherein the step (d) is carried out simultaneously with step (c), and wherein an amount of impurity ion-implanted in a region where the first resistance element is to be formed is greater than an amount of impurity ion-implanted in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

19. (previously presented) A method for manufacturing a semiconductor device according to claim 15, wherein the etching a portion of the second conducting layer also forms a first resistance element and a second resistance element in the analog element region.

20. (previously presented) A method as in claim 19, further comprising performing at least one ion-implantation of an impurity into part of the second conducting layer prior to the etching a portion of the second conducting layer.

21. (previously presented) A method as in claim 20, wherein a number of ion-implantations of impurity in a region where the first resistance element is to be formed is greater than a number of ion-implantations of impurity in a region where the second resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

22. (previously presented) A method as in claim 19, wherein, prior to the etching a portion of the second conducting layer, an impurity is diffused in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

23. (previously presented) A method as in claim 19, wherein prior to the etching a portion of the second conducting layer, a silicide layer is formed in a region where the first resistance element is to be formed so that a resistance value of the first resistance element is lower than a resistance value of the second resistance element.

24. (canceled)

25. (previously presented) A method for manufacturing a semiconductor device, the semiconductor device having a DRAM including a first capacitor formed in a DRAM region of a semiconductor substrate, and a second capacitor formed in an analog element region of the semiconductor substrate, the method comprising:

providing a DRAM region on a semiconductor substrate;

providing an analog element region on the semiconductor substrate;

simultaneously forming a first electrode for a first capacitor in the DRAM region and a second electrode for a second capacitor in the analog region by forming a first conducting layer

D1

on a dielectric layer extending from the DRAM region into the analog region and then etching a portion of the first conducting layer to define the first electrode and the second electrode, wherein the first electrode is spaced a distance away from the second electrode;

simultaneously forming a first capacitor dielectric on the first electrode for the first capacitor in the DRAM region and the second capacitor dielectric on the second electrode in the analog region by forming a dielectric layer on the first electrode and the second electrode, and etching a portion of the dielectric layer to define the first capacitor dielectric and the second capacitor dielectric, wherein the first capacitor dielectric is spaced apart from the second capacitor dielectric; and

simultaneously forming a third electrode for the first capacitor in the DRAM region and a fourth electrode for the second capacitor in the analog region by forming a second conducting layer on the first capacitor dielectric and the second capacitor dielectric and etching a portion of the second conducting layer to define the third electrode for the first capacitor and the fourth electrode for the second capacitor, wherein the first capacitor in the DRAM region comprises the first capacitor dielectric positioned between the first electrode and the third electrode, wherein the second capacitor in the analog region comprises the second capacitor dielectric positioned between the second electrode and the fourth electrode, and wherein the first capacitor is spaced a distance away from the second capacitor.

26. (previously presented) A method as in claim 25, further comprising forming the first capacitor above an upper surface of the semiconductor substrate.